

Fig. 1 (Prior Art)

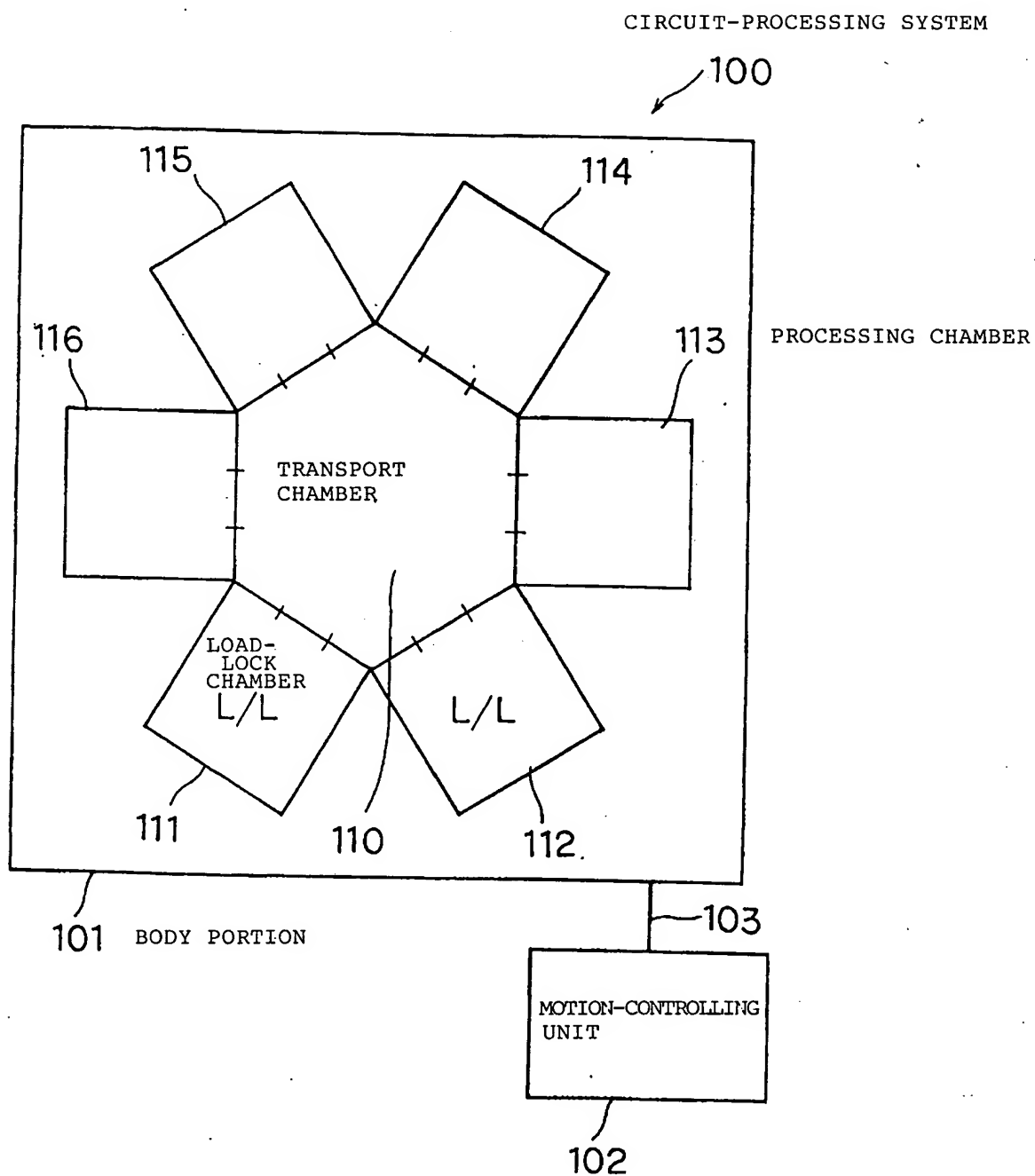
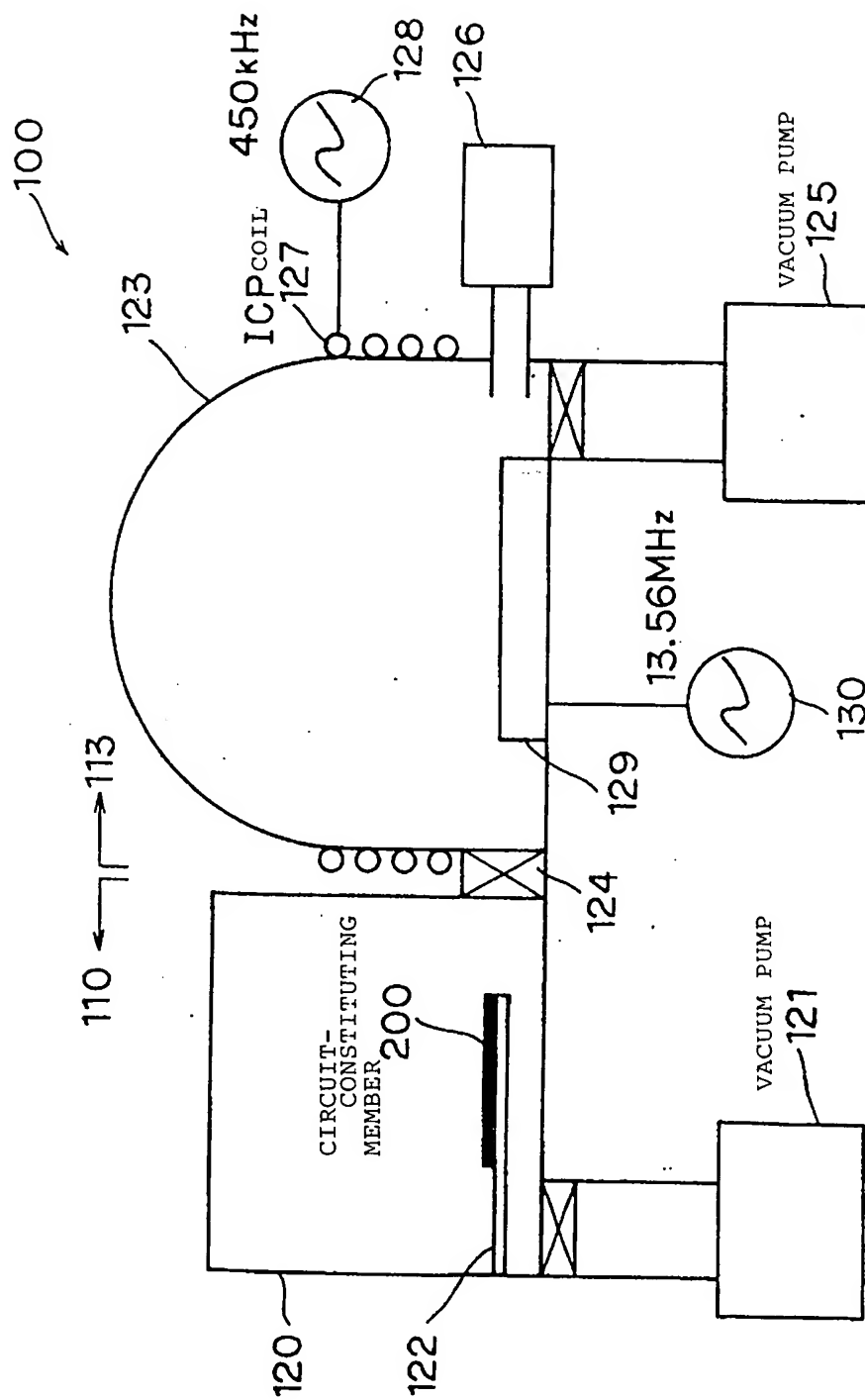


Fig. 2 (Prior Art)



(a) Cross-sectional view of an LSI device 201. It shows a substrate 210 with a MOSFET 202. The MOSFET 202 has a gate 211, a source 212, and a drain 213. A layer 216 is on top of the MOSFET. Two vertical interconnects 204 and 205 are shown, with pads 207 and 208 on top. A layer 214 is between the pads and the interconnects. A layer 215 is on top of the pads.

(b) Cross-sectional view of the LSI device 201. It shows a substrate 210 with a MOSFET 202. The MOSFET 202 has a gate 211, a source 212, and a drain 213. A layer 216 is on top of the MOSFET. A vertical interconnect 203 is shown, with a pad 206 on top. A layer 215 is on top of the MOSFET, and a layer 204 is on top of the interconnect.

· (a)

(b)

Fig. 4 (Prior Art)

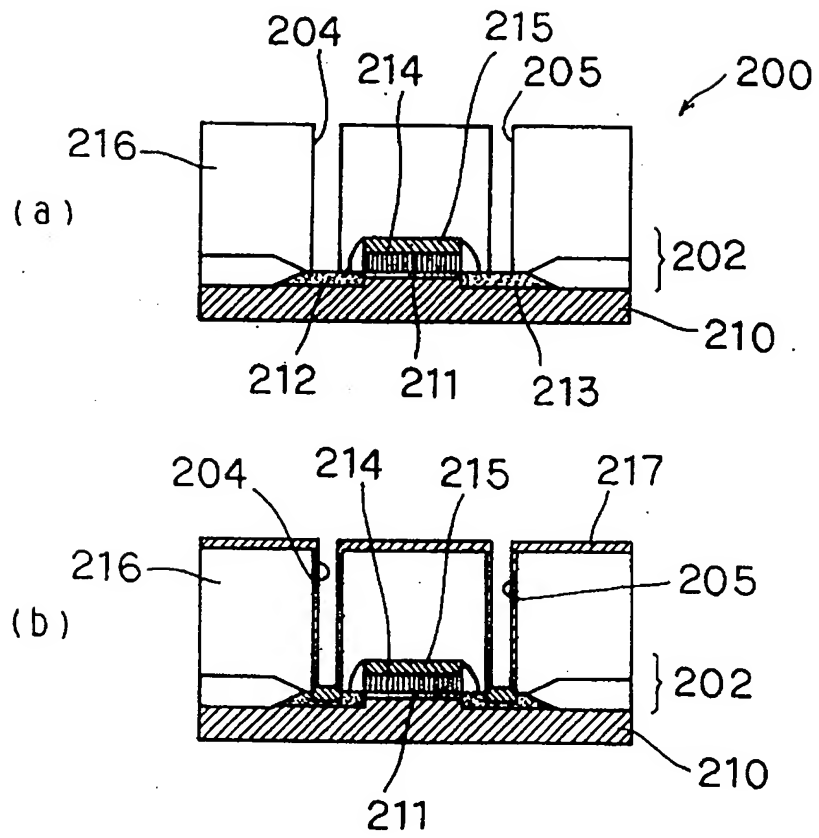


Fig. 5 (Prior Art)

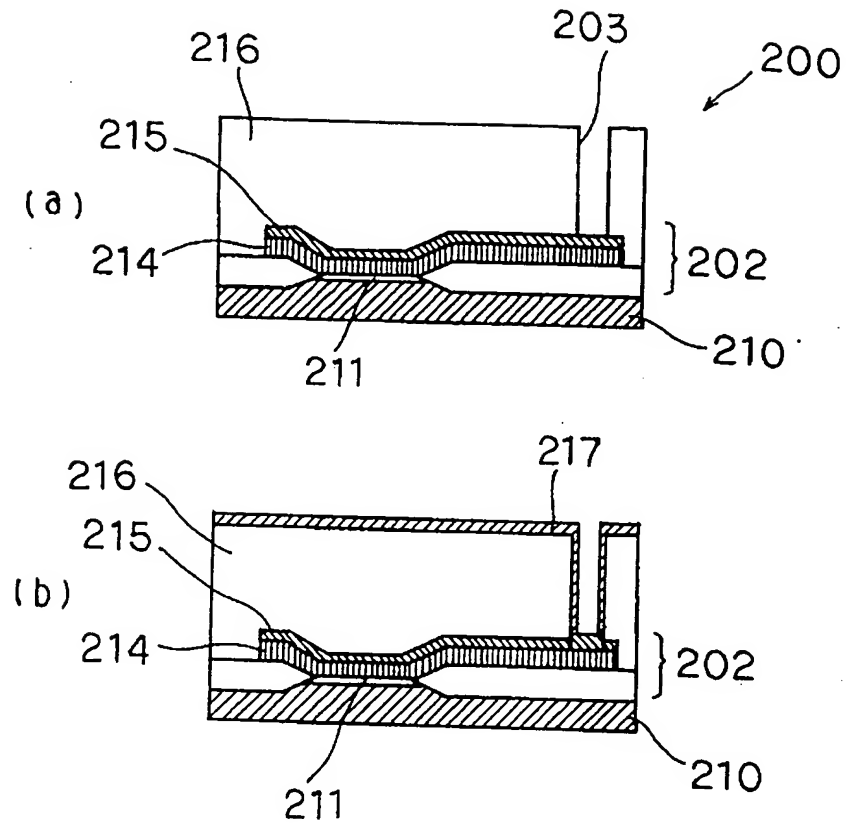


Fig. 6 (Prior Art)

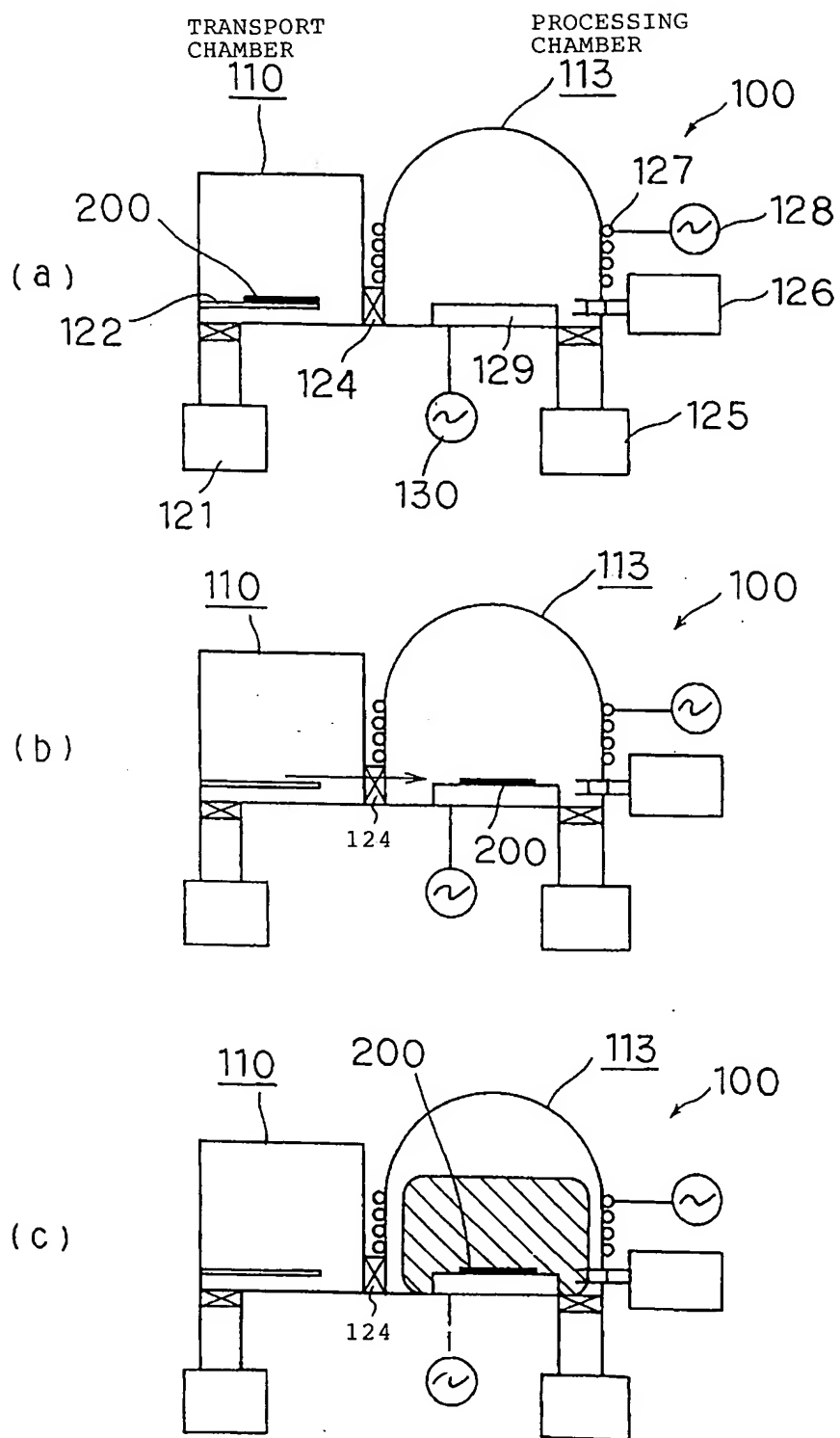


Fig. 7 (Prior Art)

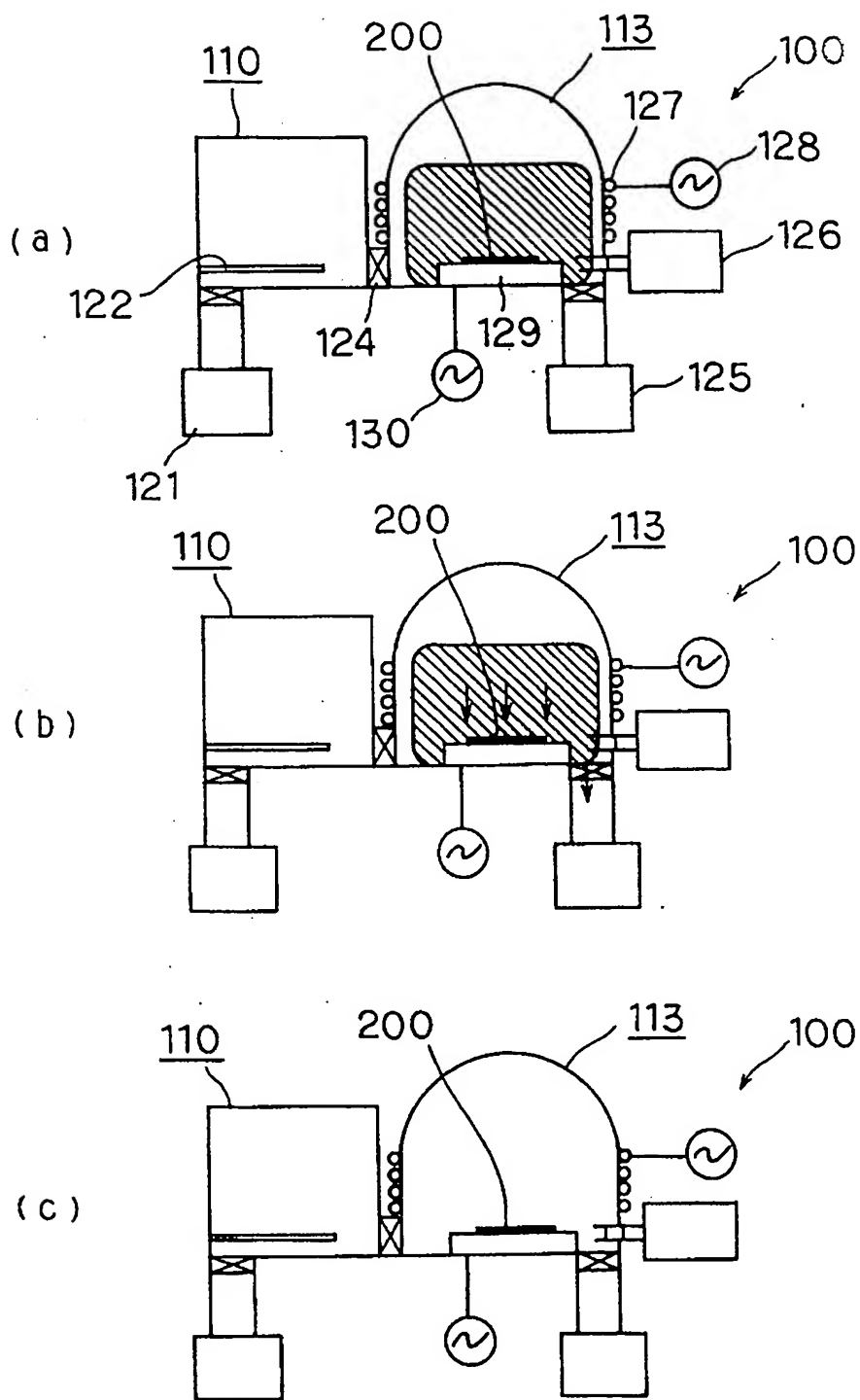


Fig. 8 (Prior Art)

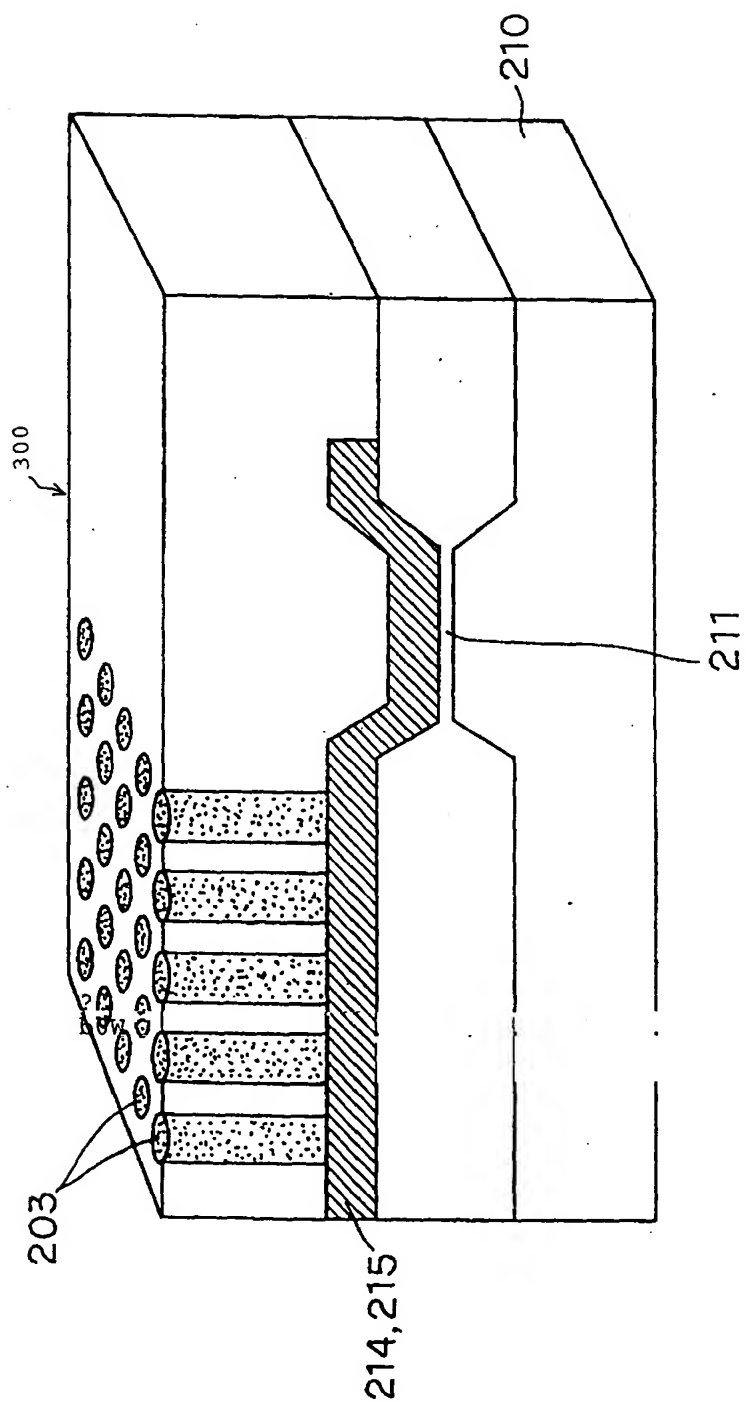


Fig. 9 (Prior Art)

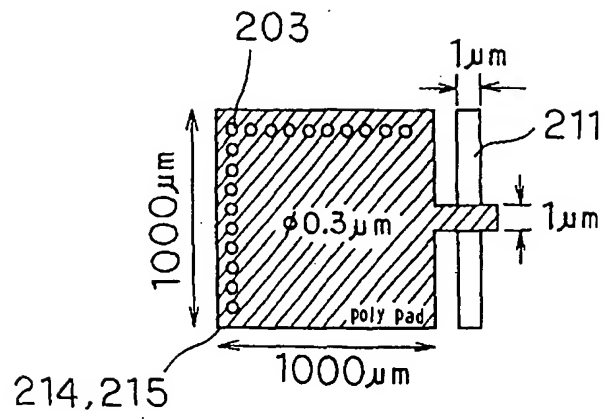


Fig. 10 (Prior Art)

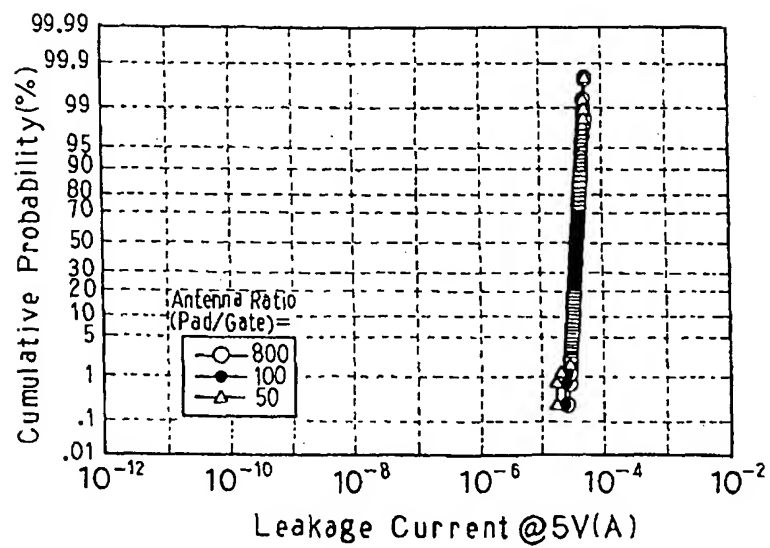


Fig. 11

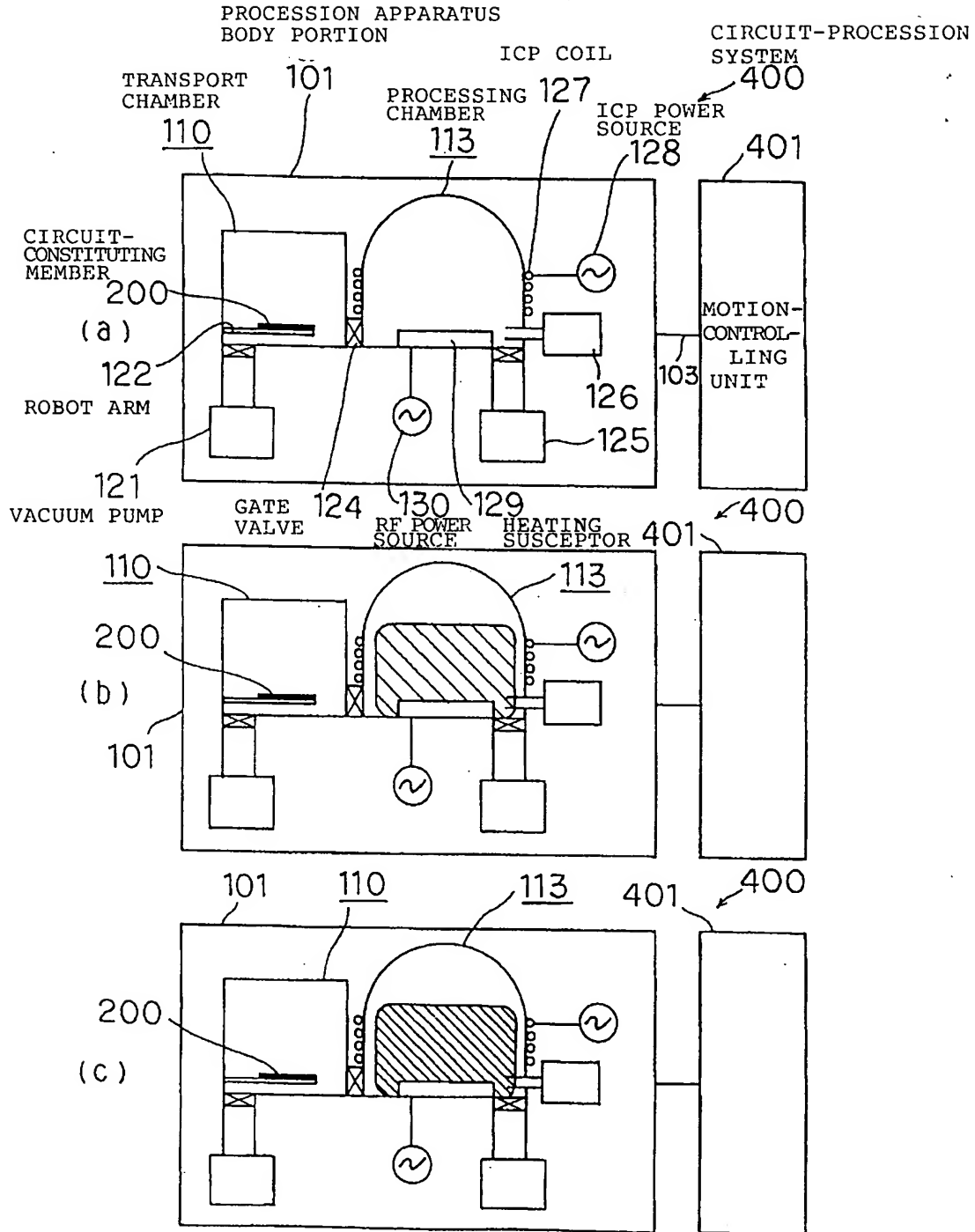


Fig. 12

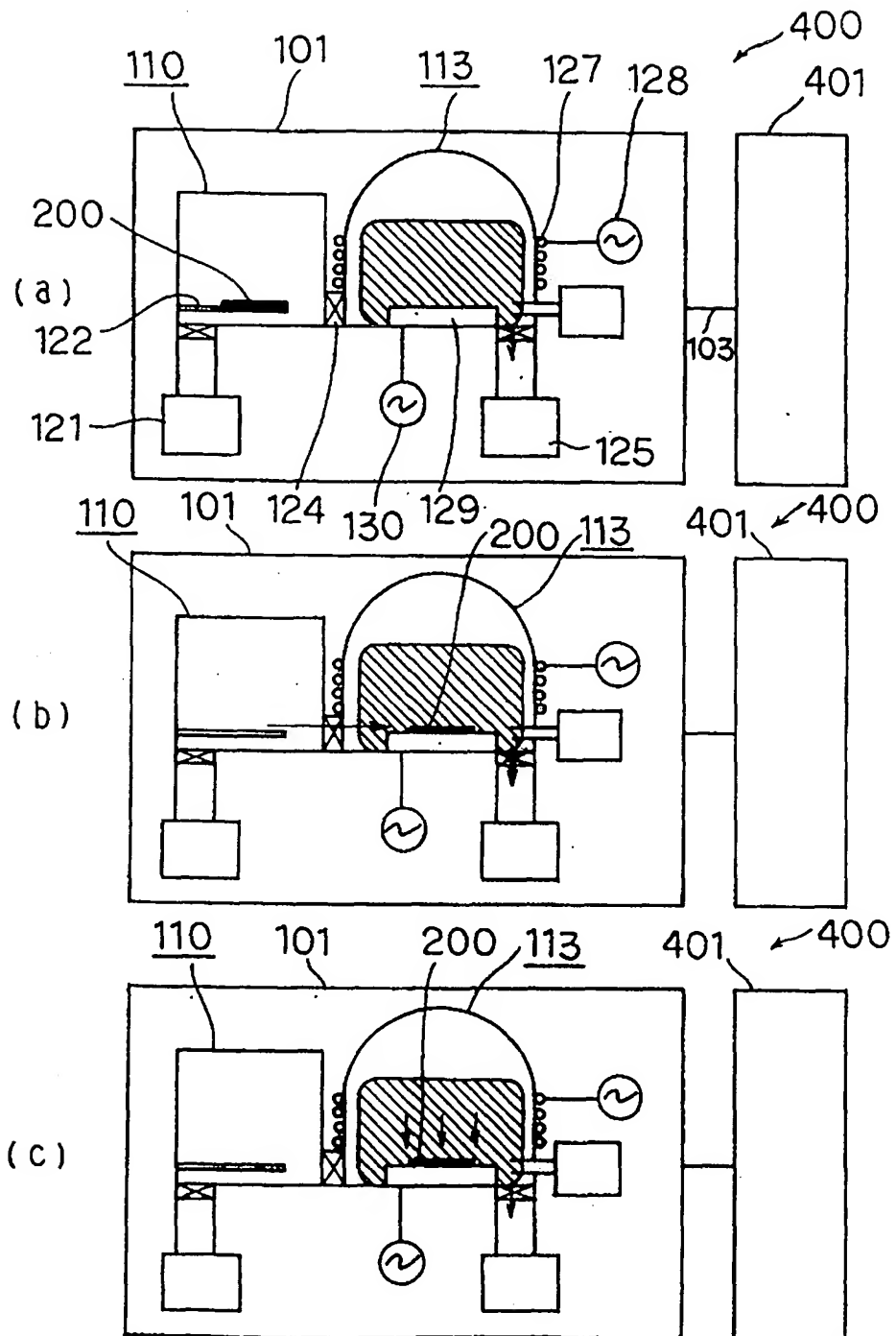


Fig. 13

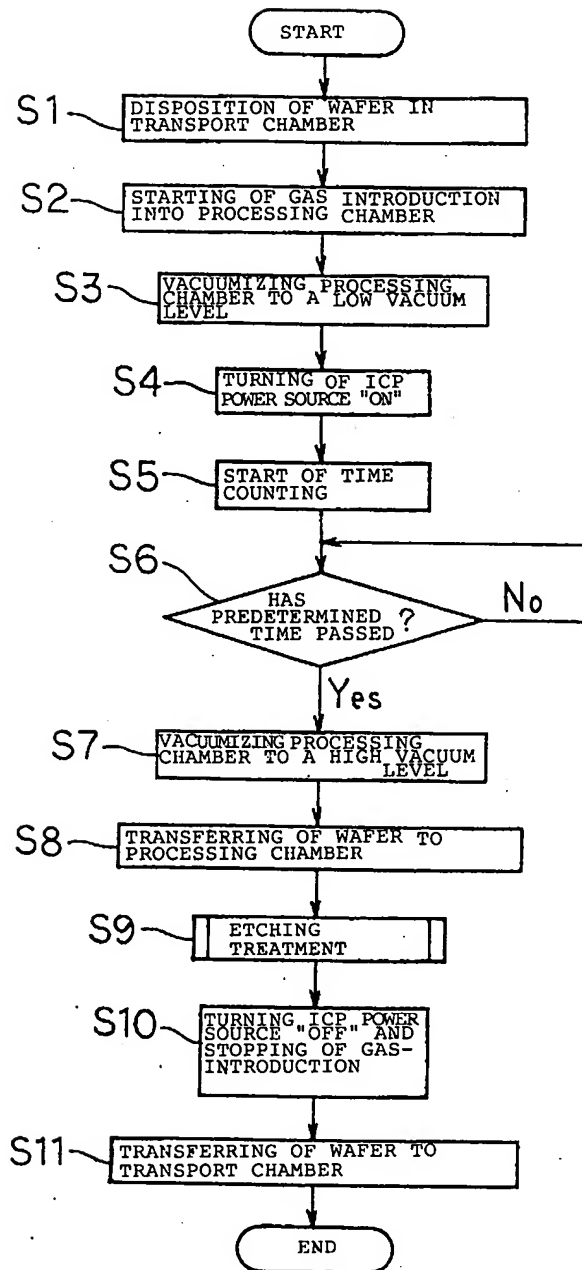


Fig. 14

